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March 4, 2008

AMENDMENTS TO THE CLAIMS:

Please amend claims 1-24, 26-36 and 38-48 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) Apparatus for processing data comprising:

processing logic operable to perform data processing operations; and

an instruction decoder for decoding program instructions to control said processing logic to perform data processing operations specified by said program instructions, wherein said instruction decoder, in response to a compare and branch instruction, comprises a decoder for:

(i) performing a comparison between a first value stored in a first register and a second value stored in a second register;

(ii) for copying, in dependence upon a result of said comparison, a program counter value to a third register;

(iii) for determining a target branch address from a pre-programmed stored value and said program counter value; and

(iv) for branching to a sub-routine at said target branch address in dependence upon a result of said comparison.

2. (currently amended) ApparatusThe apparatus as claimed in claim 1, wherein said instruction is an array bounds checking instruction and said sub-routine is an array bounds exception handling routine.

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3. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 1, wherein at least

one of said first register and said second register are specified within said compare and branch

instruction.

4. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 2, wherein said first

value is a reference value specifying an array size and said second value is a test value

determined from a decoded program instruction.

5. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 4, wherein said

comparison determines whether said reference value is greater than or equal to said test value.

6. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 4, wherein said result

of said comparison is determined from a carry flag value and zero flag value.

7. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 2, wherein said

branching operation comprises copying a pointer to said array bounds exception handling routine

into a register specifying a next program instruction.

8. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 1, wherein said data

processing apparatus comprises a co-processor and said pre-programmed stored value is read

from a register of said co-processor.

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9. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 1, wherein said compare and branch instruction is executed within a single processing cycle of said data processing apparatus when the branch is not taken.

10. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 1, wherein said instruction decoder is operable to decode translated platform-independent program instructions.

11. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 10, wherein said platform independent program instructions are one of :

Java bytecodes;

.net bytecodes;

MSIL bytecodes; and

CIL bytecodes.

12. (currently amended) ~~Apparatus~~The apparatus as claimed in claim 1, wherein said data processing apparatus is operable in a user mode and a privileged mode and said data processing apparatus remains in said user mode during execution of said compare and branch instruction.

13. (currently amended) A method of processing data with an apparatus for processing data having processing logic operable to perform data processing operations and an instruction decoder operable to decode a compare and branch instruction to control said processing logic to perform data processing operations specified by said program instructions, said method comprising the steps of:

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(i) performing a comparison between a first value stored in a first register and a second value stored in a second register;

(ii) copying a program counter value, in dependence upon said comparison, to a third register;

(iii) to determinedetermining a target branch address from a pre-programmed stored value and said program counter value; and

(iv) to branchbranching to a sub-routine at said target branch address in dependence upon a result of said comparison.

14. (currently amended) AThe method as claimed in claim 13, wherein said instruction is an array bounds checking instruction and said sub-routine is an array bounds exception handling routine.

15. (currently amended) AThe method as claimed in claim 13, wherein at least one of said first register and said second register are specified within said compare and branch instruction.

16. (currently amended) AThe method as claimed in claim 14, wherein said first value is a reference value specifying an array size and said second value is a test value determined from a decoded program instruction.

17. (currently amended) AThe method as claimed in claim 16, wherein said comparison determines whether said reference value is greater than or equal to said test value.

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18. (currently amended) A~The method as claimed in claim 16, wherein said result of said comparison is determined from a carry flag value and a zero flag value.

19. (currently amended) A~The method as claimed in claim 14, wherein said branching operation comprises copying a pointer to said array bounds exception handling routine into a register specifying a next program instruction.

20. (currently amended) A~The method as claimed in claim 13, wherein said data processing apparatus comprises a co-processor and said pre-programmed stored value is read from a register of said co-processor.

21. (currently amended) A~The method as claimed in claim 13, wherein said compare and branch instruction is executed within a single processing cycle of said data processing apparatus when the branch is not taken.

22. (currently amended) A~The method as claimed in claim 13, wherein said instruction decoder is operable to decode translated platform-independent program instructions.

23. (currently amended) A~The method as claimed in claim 22, wherein said platform independent program instructions are one of :

Java bytecodes;

.net bytecodes;

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MSIL bytecodes; and

CIL bytecodes.

24. (currently amended) AThe method as claimed in claim 13, wherein said data
processing apparatus is operable in a user mode and a privileged mode and said data processing
apparatus remains in said user mode during execution of said compare and branch instruction.

25. (previously presented) A computer program product comprising a computer-readable
storage medium including a computer program operable to control an apparatus for processing
data having processing logic operable to perform data processing operations and an instruction
decoder operable to decode a compare and branch instruction to control said processing logic to
perform data processing operations specified by said program instructions, said computer
program comprising the steps of:

(i) performing a comparison between a first value stored in a first register and a second
value stored in a second register;

(ii) copying a program counter value, in dependence upon said comparison, to a third
register;

(iii) determining a target branch address from a pre-programmed stored value; and

(iv) branching to a sub-routine at said target branch address in dependence upon a result
of said comparison.

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26. (currently amended) A̶The computer program product as claimed in claim 25, wherein said instruction is an array bounds checking instruction and said sub-routine is an array bounds exception handling routine.

27. (currently amended) A̶The computer program product as claimed in claim 25, wherein at least one of said first register and said second register are specified within said compare and branch instruction.

28. (currently amended) A̶The computer program product as claimed in claim 26, wherein said first value is a reference value specifying an array size and said second value is a test value determined from a decoded program instruction.

29. (currently amended) A̶The computer program product as claimed in claim 28, wherein said comparison determines whether said reference value is greater than or equal to said test value.

30. (currently amended) A̶The computer program product as claimed in claim 28, wherein said result of said comparison is determined from a carry flag value and a zero flag value.

31. (currently amended) A̶The computer program product as claimed in claim 26, wherein said branching operation comprises copying a pointer to said array bounds exception handling routine into a register specifying a next program instruction.

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32. (currently amended) A The computer program product as claimed in claim 25,

wherein said data processing apparatus comprises a co-processor and said pre-programmed

stored value is read from a register of said co-processor.

33. (currently amended) A The computer program product as claimed in claim 25,

wherein said compare and branch instruction is executed within a single processing cycle of said

data processing apparatus when the branch is not taken.

34. (currently amended) A The computer program product as claimed in claim 25,

wherein said instruction decoder is operable to decode translated platform-independent program

instructions.

35. (currently amended) A The computer program product as claimed in claim 34,

wherein said platform independent program instructions are one of:

  Java bytecodes;

  .net bytecodes;

  MSIL bytecodes; and

  CIL bytecodes.

36. (currently amended) A The computer program product as claimed in claim 25,

wherein said data processing apparatus is operable in a user mode and a privileged mode and

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said data processing apparatus remains in said user mode during execution of said compare and

branch instruction.

37. (previously presented) A computer program product comprising a computer-readable

storage medium including a computer program operable to translate non-native program

instructions to form native program instructions directly decodable by an apparatus for

processing data having processing logic operable to perform data processing operations and an

instruction decoder operable to decode a compare and branch instruction to control said

processing logic to perform data processing operations specified by said program instructions,

said native program instructions comprising:

(i) performing a comparison between a first value stored in a first register and a second

value stored in a second register;

(ii) copying a program counter value, in dependence upon said comparison, to a third

register;

(iii) determining a target branch address from a pre-programmed stored value; and

(iv) branching to a sub-routine at said target branch address in dependence upon a result

of said comparison.

38. (currently amended) AThe computer program product as claimed in claim 37,

wherein said instruction is an array bounds checking instruction and said sub-routine is an array

bounds exception handling routine.

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39. (currently amended) A The computer program product as claimed in claim 37,
wherein at least one of said first register and said second register are specified within said
compare and branch instruction.

40. (currently amended) A The computer program product as claimed in claim 38,
wherein said first value is a reference value specifying an array size and said second value is a
test value determined from a decoded program instruction.

41. (currently amended) A The computer program product as claimed in claim 40,
wherein said comparison determines whether said reference value is greater than or equal to said
test value.

42. (currently amended) A The computer program product as claimed in claim 40,
wherein said result of said comparison is determined from a carry flag value and a zero flag
value.

43. (currently amended) A The computer program product as claimed in claim 38,
wherein said branching operation comprises copying a pointer to said array bounds exception
handling routine into a register specifying a next program instruction.

44. (currently amended) A The computer program product as claimed in claim 37,
wherein said data processing apparatus comprises a co-processor and said pre-programmed
stored value is read from a register of said co-processor.

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45. (currently amended) AThe computer program product as claimed in claim 37,

wherein said compare and branch instruction is executed within a single processing cycle of said

data processing apparatus when the branch is not taken.

46. (currently amended) AThe computer program product as claimed in claim 37,

wherein said instruction decoder is operable to decode translated platform-independent program

instructions.

47. (currently amended) AThe computer program product as claimed in claim 46,

wherein said platform independent program instructions are one of :

    Java bytecodes;

    .net bytecodes;

    MSIL bytecodes; and

    CIL bytecodes.

48. (currently amended) AThe computer program product as claimed in claim 37,

wherein said data processing apparatus is operable in a user mode and a privileged mode and

said data processing apparatus remains in said user mode during execution of said compare and

branch instruction.

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PAGE 13/28 * RCVD AT 3/4/2008 2:36:39 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-4/20 * DNIS:2738300 * CSID:703+816+4100 * DURATION (mm-ss):07-06

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AMENDMENTS TO THE DRAWINGS

Please substitute the attached five (5) sheets of replacement drawings for the drawings

originally filed.

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